AMENDMENT TO THE SPECIFICATION

Please replace the first full paragraph on page 14 with the following paragraph.

The read enable input to the FIFO memories ~~331-334~~311-314 (shown in Figure 4) are tied asserted high as shown at 504, 507, 510, and 513. The read addresses for FIFO memories ~~331-334~~311-314 are initial set to zero as shown at 505, 508, 511, and 514. In this example, it takes the system 2 clock cycles to prepare the requested data for output. Data 0 is ready for output at FIFO memory ~~331~~311 at time 3 as shown at 506. Similarly, data 1-3 are also ready for output at FIFO memories ~~332-334~~312-314 at time 3, as shown at 509, 512, and 515, since they were requested at the same time as data 0.

Please replace the second full paragraph on page 14 with the following paragraph.

When the data reading device transmits a read address to request data 0 at time 3 as shown at 503, this triggers the next read address in FIFO memory ~~331~~311 to be asserted at time 4 as shown at 505. The data associated with that address (data 4) at FIFO memory ~~331~~311 is ready for output at time 6 as shown at 506.

Please replace the third full paragraph on page 14 with the following paragraph.

When the data reading device transmits a read address to request data 1 at time 4 as shown at 503, this triggers the next read address in FIFO memory ~~332~~312 to be asserted at time 5 as shown at 508. The data associated with that address (data 5) at FIFO memory ~~332~~312 is ready for output at time 7 as shown at 509.

Please replace the fourth full paragraph on page 14 with the following paragraph.

When the data reading device transmits a read address to request data 2 at time 5 as shown at 503, this triggers the next read address in FIFO memory ~~333~~313 to be asserted at time 6 as shown at 511. The data associated with that address (data 6) at FIFO memory ~~333~~313 is ready for output at time 8 as shown at 512.

Please replace the fifth full paragraph on page 14 with the following paragraph.

When the data reading device transmits a read address to request data 3 at time 6 as shown at 503, this triggers the next read address in FIFO memory ~~334~~314 to be asserted at time 7 as shown at 514. The data associated with that address (data 7) at FIFO memory ~~334~~314 is ready for output at time 9 as shown at 515.